Notice of Allowability	Application No.	Applicant(s)	
	09/879,434	YOO ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed February 2, 2005*.

2. ☒ The allowed claim(s) is/are *claims 1-12, 14-17, and 19-21 renumbered respectively as claims 1-19*.

3. ☒ The drawings filed on *21 June 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050607* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. Claims 1-12, 14-17, and 19-21 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Frank V. DeRosa (43584) on June 7, 2005.

The application has been amended as follows wherein the following versions of claims 1, 3, 4, 8-10, 14, 16, 19, and 21 replace all prior versions and listings:

1. A data recovery apparatus, comprising:

a phase locked loop (PLL) for generating a plurality of phase clock signals each having a different delay time with respect to a clock signal;

an oversampler for M times oversampling serial input data in response to the plurality of phase clock signals and outputting a plurality of data bits in parallel, wherein M is an integer;

a level transition detector for receiving the parallel data bits output from the oversampler, detecting logic level transitions between successive bits of the parallel data bits and generating a detection result as one of M transition signals;

a transition accumulator for accumulating a number of times each one of the M transition signals is generated and outputting a transition accumulation signal corresponding to the transition signal whose generation frequency is highest, the transition accumulation signal comprising one of M transition accumulation signals,

wherein the transition accumulator comprises a reset signal generator for performing a logical combination of the M transition accumulation signals and

generating an accumulation reset signal for resetting the transition accumulator in response to the logical combination result;

a state selector for generating a state signal in response to the transition accumulation signal output from the transition accumulator, wherein the state signal is used for selecting corresponding data bits ~~of corresponding positions~~ among the parallel data bits output from the oversampler; and

a data selector for receiving the parallel data bits, utilizing the state signal to select from the parallel data bits those data bits having sampling positions corresponding to ~~the state of~~ the state signal, and outputting the selected data bits in parallel.

3. The data recovery apparatus of claim 2, wherein the level transition detector comprises:

a transition detector comprising a plurality of exclusive OR gates for performing an exclusive OR operation on ~~two adjacent~~ successive bits of the parallel ~~paralled~~ data bits output from the oversampler and generating exclusive OR results as first, second, and third output signals; and

a transition detection signal outputting unit for processing the first, second, and third output signals to generate and output a first, second or third transition signal as a result of said processing.

4. The data recovery apparatus of claim 3, wherein the transition accumulator comprises:

a first accumulator for accumulating the first transition signal in response to an input clock signal and outputting a first transition accumulation signal when a predetermined number of first transition signals are accumulated;

a second accumulator for accumulating the second transition signal in response to the input clock signal and outputting a second transition accumulation signal when a predetermined number of second transition signals are accumulated;

a third accumulator for accumulating the third transition signal in response to the input clock signal and outputting a third transition accumulation signal when ~~the accumulated number is~~ a predetermined number of third transition signals are accumulated; and

wherein the reset signal generator performs the logical combination on the first, second, and third transition accumulation signals and generates the accumulation reset signal for resetting the first, second, and third accumulators in response to the logical combination result.

8. The data recovery apparatus of claim 7, wherein the data selector comprises a plurality of multiplexers m(i), wherein each multiplexer receives M bits of the parallel data bits output from the oversampler and selectively outputs one bit among the received M bits in response to the state signal.

9. The data recovery apparatus of claim 8, wherein each multiplexer m(i) (i = 1, 2, 3, 4) receives the M bits of the parallel data bits at bit positions D(p) where p= (3P, 3P+1,3P+2)~~, where~~ and P= i-1, and wherein the data selector outputs the 3P+2~~th~~ bits ~~output~~ from each of the plurality of multiplexers m(i) when the state signal is "01", outputs the 3P~~th~~ bits ~~output~~ from each of the plurality of multiplexers m(i) when the state signal is "10", and outputs the 3P+1~~th~~ bits ~~output~~ from each of the plurality of multiplexers m(i) when the state signal is "00".

10. A data recovery method comprising the steps of:

(a) receiving as input serial data in blocks of K bits and performing an M times oversampling on each block of serial data using N phase clock signals having different delay times to output N data bits in parallel, wherein K, M, and N are integers;

(b) detecting a level transition between successive bits of the N data bits and generating a transition signal when ~~a~~ the level transition is detected, the transition signal comprising one of M transition signals;

(c) accumulating a number of generations of each of the M transition signals and outputting a transition accumulation signal corresponding to a transition signal whose generation frequency meets a predefined threshold, the transition accumulation signal comprising one of M transition accumulation signals;

(d) performing a logical combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the accumulating ~~process~~ step in response to the logical combination result; and

(e) selecting from the N data bits, K data bits corresponding to the transition signal whose generation frequency meets the predefined threshold.

14. The data recovery method of claim 11, wherein the N parallel data bits include bits D(i) (i=0, ... N-1) ~~in three-times-oversampling positions~~, and wherein step (e) comprises the steps of:

selecting K ~~oversampled~~ data bits from the N parallel data bits at ~~each three-times-oversampling~~ positions D(3P+2), for (P=0, ... K-1), corresponding to a first transition signal of the M transition signals when the first transition signal is the transition signal whose generation frequency meets the predefined threshold;

selecting K ~~oversampled~~ data bits from the N parallel data bits at ~~each three times-oversampling~~ positions D(3P) , for (P=0, ... K-1), corresponding to the second transition signal when the second transition signal is the transition signal whose generation frequency meets the predefined threshold; and

selecting K ~~oversampled~~ data bits from the N parallel data bits ~~at each three times-oversampling~~ positions D(3P+1), for (P=0, ... K-1), corresponding to the third transition signal when third transition signal is the transition signal whose generation frequency meets the predefined threshold.

16. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for recovering data, the method comprising the steps of:

(a) receiving as input serial data in blocks of K bits and performing an M times oversampling on each block of serial data using N phase clock signals having different delay times to output N data bits in parallel, wherein K, M, and N are integers;

(b) detecting a level transition between successive bits of the N data bits and generating a transition signal when ~~a~~ the level transition is detected, the transition signal comprising one of M transition signals;

(c) accumulating a number of generations of each of the M transition signals and outputting a transition accumulation signal corresponding to a transition signal whose generation frequency meets a predefined threshold, the transition accumulation signal comprising one of M transition accumulation signals;

(d) performing a logical combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the accumulating ~~process~~ step in response to the logical combination result; and

(e) selecting from the N data bits, K data bits corresponding to the transition signal whose generation frequency meets the predefined threshold.

19. The program storage device of claim 17, wherein the N parallel data bits include bits D(i) (i=0, ... N-1) ~~in three-times-oversampling positions~~, and wherein the instructions for performing step (e) comprise instructions for performing the steps of:

selecting K ~~oversampled~~ data bits from the N parallel data bits at ~~each three-times-oversampling~~ positions D(3P+2), for (P=0, ... K-1), corresponding to a first transition signal of the M transition signals when the first transition signal is the transition signal whose generation frequency meets the predefined threshold;

selecting K ~~oversampled~~ data bits from the N parallel data bits at ~~each three times-oversampling~~ positions D(3P) , for (P=0, ... K-1), corresponding to the second transition signal when the second transition signal is the transition signal whose generation frequency meets the predefined threshold; and

selecting K ~~oversampled~~ data bits from the N parallel data bits at ~~each three times-oversampling~~ positions D(3P+1), for (P=0, ... K-1), corresponding to the third

transition signal when third transition signal is the transition signal whose generation frequency meets the predefined threshold.

21. A circuit for recovering data, the circuit comprising:

a first circuit for performing an M times oversampling on a block of input serial data using N phase clock signals having different delay times and outputting N data bits in parallel, wherein M and N are integers;

a second circuit for detecting a level transition between successive bits of the N data bits and generating a transition signal when a level transition is detected, the transition signal comprising one of M transition signals;

a third circuit for accumulating a number of generations of each of the M transition signals and outputting a transition accumulation signal corresponding to a transition signal whose generation frequency meets a predefined threshold, the transition accumulation signal comprising one of M transition accumulation signals;

a fourth circuit for performing a logical combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the accumulating process in response to the logical combination result; and

a fifth circuit for selecting from the N data bits, K data bits corresponding to the transition signal whose generation frequency meets the predefined threshold, wherein K is an integer.

Claims 1-12, 14-17, and 19-21 are renumbered respectively as claims 1-19, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

3. Claims 1-12, 14-17, and 19-21 renumbered respectively as claims 1-19 are allowed.

4. Claims 1-12, 14-17, and 19-21 renumbered respectively as claims 1-19 are allowed because the prior art of record does not disclose, as indicated in the first office action, the reset generator for performing a logical combination of the transition accumulation signals to reset the transition accumulator.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
June 7, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER